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April 19, 2004

MAIL STOP DD
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: App No. 10/804,452; "Memory Expansion and Integrated Circuit Stacking
System and Method"
Docket No. 0254-094-PCT-2-C1

Dear Commissioner:

Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 102 references; and
4. a return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP

A handwritten signature in black ink, appearing to read "Pam Menke".

Pam Menke
Board Certified Legal Assistant in Civil Trial Law
Texas Board of Legal Specialization

/pm
enclosures



Attorney Docket No.: 0254-094-PCT-2-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Memory Expansion and Integrated Circuit Stacking System and Method
Application No.: 10/804,452
Filing Date: 03/19/2004
Inventor: Russell Rapport, et al.
Assignee: Staktek Group, L.P.
Examiner: TBA
Group: TBA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (six sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

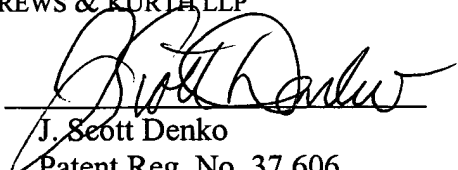


This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. A duplicate copy of Form 1449 is enclosed.

Respectfully submitted,

ANDREWS & KURTH LLP

April 19, 2004
Date

By: 
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Form PTO-1449 (Modified)
(Rev. 11/92)U.S. Dept. of Commerce
Patent and Trademark Office

ATTY. DOCKET NO.

SERIAL NO.

0254-094-PCT-2-C1

10/804,452

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

(37 CFR 1.98(b))

APPLICANT

Rapport, et al

FILING DATE

3/19/04

GROUP

U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No

OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

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						Yes	No
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					Yes	No
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/	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.
/	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
/	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
/	Teresa Technologies, Inc. – Semiconductor Intellectual Property, Chip Scale Packaging – Website pages (3)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)									
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	Document Number	Date	Country	Class	Subclass	Translation			
						Yes	No		
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	Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.								
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	"Vertically-Intergrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University								
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FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

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					Yes	No

OTHER DOCUMENTS

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

5	Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5
✓	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams

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